

In the Claims:

The claims are as follows:

1. (Previously Presented) An integrated circuit device, comprising:

a first power rail for supplying power to a first latch and a circuit only during a first clock phase, said first power rail supplied from a first power supply;

a second power rail for supplying power to a second latch only during a second clock phase, said second power rail supplied from a second power supply; and

said circuit coupled between an output of said first latch and an input of said second latch.

2. (Original) The integrated circuit device of claim 1, further comprising a second circuit coupled to an output of said second latch and powered from said second rail.

3. (Previously Presented) The integrated circuit device of claim 1, wherein said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock, said first and second clocks powered from a third power rail, said third power rail supplied from a third power supply.

4. (Original) The integrated circuit device of claim 1, wherein:

said first power rail is powered before said first clock phase goes high and is de-powered after said first clock phase goes low; and

said second power rail is powered before said second clock phase goes high and is de-powered after second first clock phase goes low.

5. (Original) The integrated circuit device of claim 1, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

6. (Previously Presented) An integrated circuit device, comprising:

a first power rail for supplying power to an L1 latch of an L1/L2 latch only during a first clock phase, said first power rail supplied from a first power supply; and
a second power rail for supplying power to an L2 latch of said L1/L2 latch and to a circuit coupled to an output of said L2 latch only during a second clock phase, said second power rail supplied from a second power supply.

7. (Original) The integrated circuit device of claim 6, further comprising a second L1/L2 latch wherein said circuit is coupled to an input of an L1 latch of said second L1/L2 latch, said L1 latch of said second L1/L2 latch powered by said first power rail and an L2 latch of said second L1/L2 latch powered by said second power rail.

8. (Previously Presented) The integrated circuit device of claim 6, wherein said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock, said first and second clocks powered from a third power rail, said third power rail supplied from a third power supply.

9. (Original) The integrated circuit device of claim 6, wherein:

said first power rail is powered before said first clock phase goes high and is de-powered after said first clock phase goes low; and
said second power rail is powered before said second clock phase goes high and is de-powered after second first clock phase goes low.

10. (Original) The integrated circuit device of claim 6, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

11. (Previously Presented) An integrated circuit device, comprising:

a first power rail for supplying power to first latch and a first circuit only during a first clock phase, said first power rail supplied from a first power supply;
a second power rail for supplying power to a second latch and a second circuit only during a second clock phase, said second power rail supplied from a second power supply;
a third power rail for supplying power to a third latch and a third circuit only during a third clock phase, said third power rail supplied from a third power supply;
a fourth power rail for supplying power to fourth latch and a fourth circuit only during a fourth clock phase, said fourth power rail supplied from a fourth power supply; and
said first circuit coupled between an output of said first latch and an input of said second latch, said second circuit coupled between an output of said second latch and an input of said

third latch, said third circuit coupled between an output of said third latch and an input of said fourth latch and said fourth circuit coupled to an output of said fourth latch.

12. (Original) The integrated circuit device of claim 11, further comprising a fifth latch powered from said first power rail, said fourth circuit coupled to an input of said fifth latch.

13. (Previously Presented) The integrated circuit device of claim 11, wherein said first clock phase is supplied from a first clock, said second clock phase is supplied from a second clock, said third clock phase is supplied from a third clock and said fourth clock phase is supplied from a fourth clock, said first, second, third and fourth clocks powered from a fifth power rail, said fifth power rail supplied from a fifth power supply.

14. (Original) The integrated circuit device of claim 11, wherein:

 said first power rail is powered before said first clock phase goes high and is de-powered after said first clock phase goes low;

 said second power rail is powered before said second clock phase goes high and is de-powered after second first clock phase goes low;

 said third power rail is powered before said third clock phase goes high and is de-powered after said third clock phase goes low; and

 said fourth power rail is powered before said fourth clock phase goes high and is de-powered after second first clock phase goes low.

15. (Original) The integrated circuit device of claim 11, whercin only one of said first clock phase, second clock phase, third clock phase and fourth clock phase is high at a time.

16. (Original) The integrated circuit of claim 15, wherein said second clock phase goes high when said first clock phase goes low, said third clock phase goes high when said second clock phase goes low, said fourth clock phasc goes high when said third clock phase goes low and said first clock phase goes high when said fourth clock phase goes low.

17. (Previously Presented) A method of stressing an integrated circuit, comprising:

providing said integrated circuit, said integrated circuit including a first power rail for supplying power to first latch and a circuit, a second power rail for supplying power to a second latch, and said circuit coupled between an output of said first latch and an input of said second latch;

powering said first power rail only during each phase of a first clock, said first power rail supplied from a first power supply; and

powering said second power rail during each phase of a second clock, said second power rail supplied from a second power supply.

18. (Original) The method of claim 17, further comprising a second circuit coupled to an output of said second latch and powered from said second rail.

19. (Previously Presented) The method of claim 17,whercin:

said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock; and
powering said first and second clocks from a third power rail, said third power rail supplied from a third power supply.

20. (Original) The method of claim 17, further including:

powering said first power rail before said first clock phase goes high and de-powering said first power rail after said first clock phase goes low; and
powering second power rail before said second clock phase goes high and de-powering said second rail after second first clock phase goes low.

21. (Original) The method of claim 17, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

22. (Previously Presented) A method of stressing an integrated circuit, comprising:

providing said integrated circuit, said integrated circuit comprising a first power rail for supplying power to an L1 latch of an L1/L2 latch; and a second power rail for supplying power to an L2 latch of said L1/L2 latch and to a circuit coupled to an output of said L2 latch;
powering said first power rail only during each phase of a first clock, said first power rail supplied from a first power supply; and
powering said second power rail only during each phase of a second clock, said second power rail supplied from a second power supply.

23. (Original) The method of claim 22, said circuit further comprising a second L1/L2 latch, said circuit coupled to an input of an L1 latch of said second L1/L2 latch, said L1 latch of said second L1/L2 latch powered by said first power rail and an L2 latch of said second L1/L2 latch powered by said second power rail.

24. (Previously Presented) The method of claim 22, wherein said first clock phase is supplied from a first clock and said second clock phase is supplied from a second clock, said first and second clocks are powered from a third power rail, said third power rail supplied from a third power supply.

25. (Original) The method of claim 22, further including:

powering said first power rail before said first clock phase goes high and de-powering said first power rail after said first clock phase goes low; and
powering said second power rail before said second clock phase goes high and de-powering said second power rail after second first clock phase goes low.

26. (Original) The method of claim 22, wherein said first clock phase is high when said second clock phase is low and said second clock phase is high when said first clock phase is low.

27. (Previously Presented) A method of stressing an integrated, comprising:

providing said integrated circuit, said integrated circuit comprising a first power rail for supplying power to first latch and a first circuit, a second power rail for supplying power to a second latch and a second circuit, a third power rail for supplying power to a third latch and a

third circuit, a fourth power rail for supplying power to fourth latch and a fourth circuit, and said first circuit coupled between an output of said first latch and an input of said second latch, said second circuit coupled between an output of said second latch and an input of said third latch, said third circuit coupled between an output of said third latch and an input of said fourth latch and said fourth circuit coupled to an output of said fourth latch;

powering said first power rail only during each phase of a first clock, said first power rail supplied from a first power supply;

powering said second power rail only during each phase of a second clock, said second power rail supplied from a second power supply;

powering said third power rail only during each phase of a third clock, said third power rail supplied from a third power supply; and

powering said fourth power rail only during each phase of a fourth clock, said fourth power rail supplied from a fourth power supply.

28. (Original) The method of claim 27, said integrated circuit further comprising a fifth latch powered from said first power rail, said fourth circuit coupled to an input of said fifth latch.

29. (Previously Presented) The method of claim 27, wherein:

said first clock phase is supplied from a first clock, said second clock phase is supplied from a second clock, said third clock phase is supplied from a third clock and said fourth clock phase is supplied from a fourth clock; and

powering said first, second, third and fourth clocks from a fifth power rail, said fifth power rail supplied from a fifth power supply.

30. (Original) The method of claim 27, further including:

powering said first power rail before said first clock phase goes high and de-powering
said first power rail after said first clock phase goes low;
powering said second power rail before said first clock phase goes high and de-powering
said second power rail after said first clock phase goes low;
powering said third power rail before said first clock phase goes high and de-powering
said third power rail after said first clock phase goes low; and
powering said fourth power rail before said first clock phase goes high and de-powering
said fourth power rail after said first clock phase goes low.

31. (Original) The method of claim 27, wherein said only one of said first clock phase, said
second clock phase, said third clock phase and fourth clock phase is high at a time.

32. (Original) The method of claim 31, wherein said second clock phase goes high when said
first clock phase goes low, said third clock phase goes high when said second clock phase goes
low, said fourth clock phase goes high when said third clock phase goes low and said first clock
phase goes high when said fourth clock phase goes low.